



STS-48/4xSTS-12 (2.5G) TO - 48 DS3 Mapper/Demapper

Product Brief
September 2003

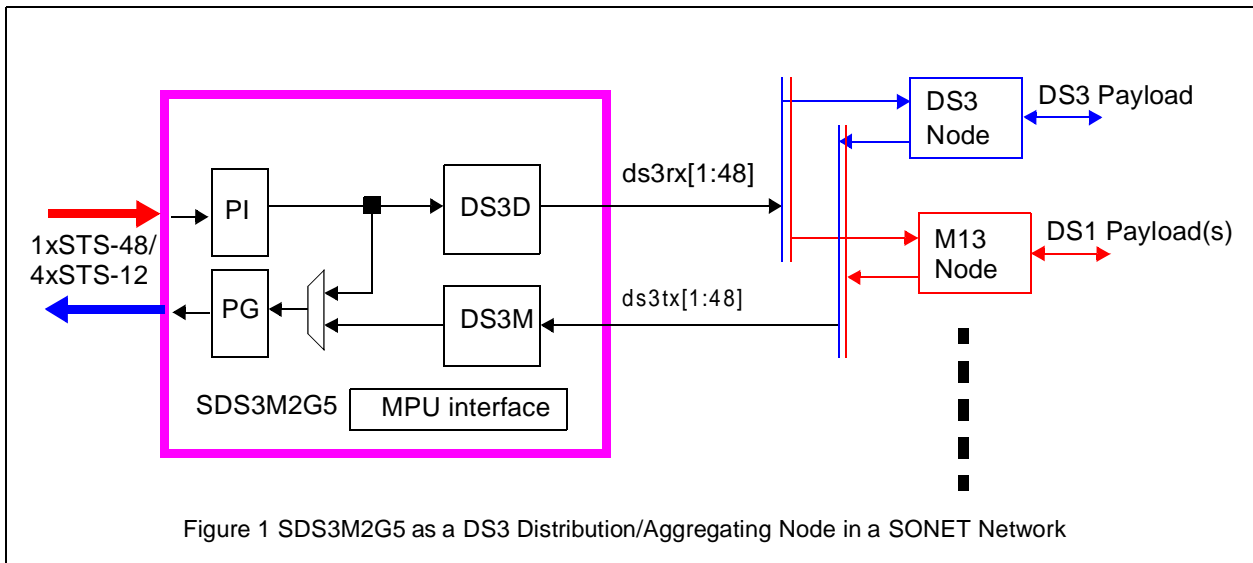
Features

- 4xSTS-12/1xSTS-48 STS-DS3 mapper and demapper
- Complaint with SONET ANSI T1.105 and GR-253-CORE
- Asynchronous DS3 mapping
- Independent 48 DS3 receive and transmit channels
- Selectable add/drop of DS3 channels
- Non-DS3 channels are looped back
- Full STS Pointer Processor
- All Line/Path overhead bytes are monitored and are regenerated
- Very small gate count
- Streamlined ASIC/FPGA portable design
- Fully synchronous design at internal 78MHz
- Can be easily upgraded to 155MHz/311MHz to reduce the gate count
- Control for external PLL for DS3 jitter attenuation in the receive side
- Data/Stuff opportunity bit output indication

- Monitoring of DS3 frames in the transmit direction
- Supports 16-bit asynchronous and synchronous microprocessor interface up to 78 MHz
- Mates seamlessly with TADM
- Delivered in Stratix or Virtex family

Applications

The SDS3M2G5 is a versatile mapper/demapper that is used to carry 48 DS3 channels in an STS-48 or 4xSTS-12 SONET streams. A typical application of SDS3M2G5 as an end-user device is shown in Figure 1. Since each of the DS3 channels are running independently they can be distributed for further mapping and demapping into DS3 clear channel, DS1, DS2 and/or DS0 payloads.



General Description

The SDS3M2G5 accepts 4xSTS-12/1xSTS-48 stream(s) in the line side. The data is framed and the line overhead bytes are monitored. The H1H2 bytes are processed by the pointer interpreter and the path overhead bytes are monitored. The individual STS1 SPEs are then passed to the transmit side or to the DS3 demapper.

The DS3 demapper extracts the DS3 payload from the STS1 SPEs and writes them to a bit FIFO. The C bits are interpreted and based on majority decision used to determine whether the S bit is a data bit or a stuff bit. The S bit interpretation is also passed to an external PLL. This PLL is used to generate the 44.736MHz DS3 clock from the 78MHz line clock. The S bit indication is used for frequency adjustments.

In the transmit direction, the received DS3 is written into a bit FIFO and is read and mapped into an STS1 SPE. Depending upon the average elastic store fill, the S bits are populated in the outgoing frame with data or stuff bit. A smooth regular insertion of stuff/data bit into the S bit is provided to reduce jitter at the far end. A functional block diagram of the SDS3M2G5 is shown in Figure 2.

Ordering and further Information

To learn more about this or any other Tip cores, contact

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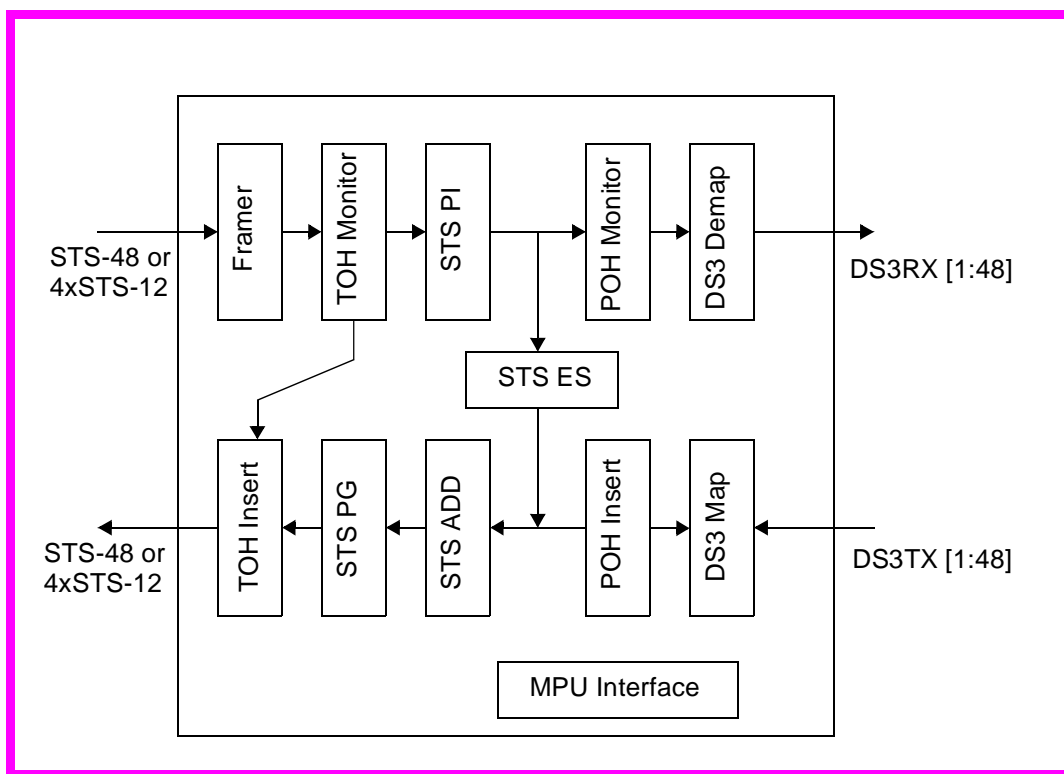


Figure 2 SDS3M2G5 Functional Block Diagram