



DS3 “e” Verification Component

The DS3 “e” Verification Component (DS3 eVC) is a package of e files for integration with an “e” verification environment.

The DS3 eVC is used to inject a DS3 formatted data into a Device UnderTest (DUT) or to monitor a DS3 formatted data from a DUT. The payload within the DS3 frame may be HDLC, ATM, or ATM PLCP formatted. ANSI T1.107-1995 specifies 3 DS3 M-frame applications. This eVC supports only the unchannelized DS3 application. This means that bit-stuffing (M23 application) and 28 DS1 channels (C-bit parity application) are not supported. The C-bit channels, however, are supported as part of the unchannelized application

Port Configuration

- The number of independent DS3 ports is user configured with a range of 1 - 255. The number of DS3 Generator Ports is independent of the number of DS3 Monitor Ports. A value of 0 turns the port off.

DS3 Generator / Monitor

- Generate/monitor a ANSI T1.107-1995 compliant DS3 signal.
- Corrupt any overhead bit on a per frame or a random basis. For example, the user can specify that 2% of DS3 frames have one of the F bits corrupted.
- Automatic framing algorithm will allow framing on a DS3 frame.
- Error reporting on any incorrect M or F bits on a per frame or a range of frames basis.
- DS3 gen./mon. interfaces with HDLC, ATM, PLCP gen./mon. to provide/verify a formatted payload.
- CP bits are automatically generated/monitored and can be corrupted.
- FEAC bits are sent as a 16-bit message.
- FEBC bits are sent as a 16-bit message.
- LAPD message is sent as a 16-bit message.
- Parity bit can be inverted on a per frame basis or over a range of frames.

HDLC Generator / Monitor

- Supports Bit-Sync Mode as defined in RFC 1662 and ISO/IEC 3309.
- Packet length is programmable and can be random.
- Select between 32-bit FCS or no FCS.
- Insert a programmable number of bit errors in the FCS field.
- Corrupt a certain percentage of packets with a variable number of FCS errors.
- Select/verify the intergap fill to be a byte or a bit. Control the length of the intergap fill. For example, can specify that the intergap fill is a random number between 15 and 200 ‘1’s.

ATM Cell Generator / Monitor

- Generate/verify ATM Cells as requested by the SPI-3 injector/collector.
- Generate/verify VPI, VCI, GFC, CLP, PTI and HEC fields.
- Optionally scramble/descramble (X**43) payload.
- Insert a user specified number of bit errors in the HEC field.
- Optionally corrupt a user specified percentage of ATM Cells with a variable number of HEC errors.

PLCP Generator / Monitor

- Generate/verify A1, A2, POI and POH bytes.
- Insert a programmable number of bit errors in of the overhead bytes.
- Calculate and report B1 errors.
- Insert a programmable number of bit errors in the B1 field.



- Follow the trailer and extract the ATM cells.
- Insert programmable/random trailer stuffing.
- Cause programmable trailer errors.

Payload Generator / Monitor

- Generate/verify payload for the HDLC, ATM and PLCP generators.
- Insert/verify header in the payload for in-band verification.
- Insert/verify destination address in the in-band header
- Insert/verify unique source address in the in-band header
- Insert/verify packet sequence number in in-band header.
- Monitor for dropped packets/cells on a channel using the sequence numbers in the in-band verification header.
- Generate/verify pattern for the payload - user can specify a fixed pattern or incrementing sequence.

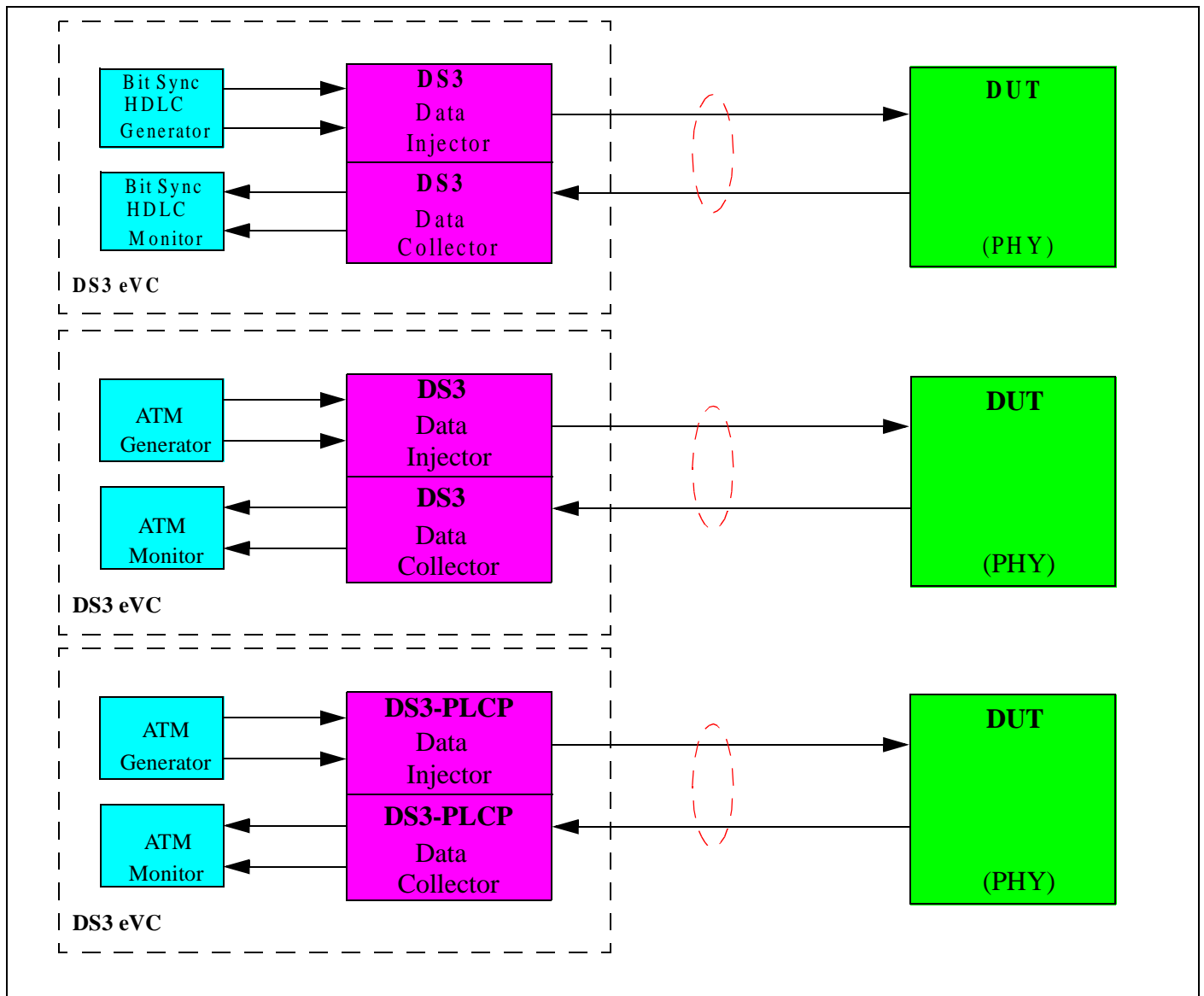


Figure 1: DS3 eVC Interface to DS3 Compliant Device Under Test (DUT)