



4xSTS12 (2.5G) STS/VT Cross Connect

Product Brief
February , 2003

Features

- 4xSTS12 STS/VT non blocking cross connect
- One working channel and one protection channel for each direction of the sonet ring
- Complaint with SONET ANSI T1.105 and GR-253-CORE
- Allows STS1, STS3c or STS12c cross connect
- Any valid configuration of VT1.5/VT2/VT3 or VT6
- Non blocking cross connect for 1344 x 1344 VT1.5 or 1008 x 1008 VT2 or 672 x 672 VT3 or 336 x 336 VT6 or any valid combination of the above
- Single chip UPSR regenerator
- Supports 1:1 Protection Switching
- Full Pointer Interpretor and Generator down to STS1 level
- Full VT Pointer Interpretor and Generator down to VT1.5/VT2/VT3/VT6 level
- Optional add/drop of STS or VT channels
- Simple 8-bit TDM bus on the system interface at 78 MHz
- Independent Line and System Clock
- All Line overhead bytes are monitored and regenerated
- Path overhead bytes of all VT enabled STS1s are monitored and regenerated
- Supports 16-byte or 64-byte J0/J1 message
- Optional monitoring/insertion of V5 byte
- Supports Near-end, Far-end STS1, Far-end VT, and System Loopbacks
- Supports 16-bit asynchronous and synchronous microprocessor interface up to 78 MHz
- Fully synchronous design at internal 78MHz
- Streamlined ASIC/FPGA portable design
- Can be easily upgraded to 155MHz/311MHz to reduce the gate count
- Mates seamless with TADM at 78MHz
- Delivered in the Stratix or Virtex family

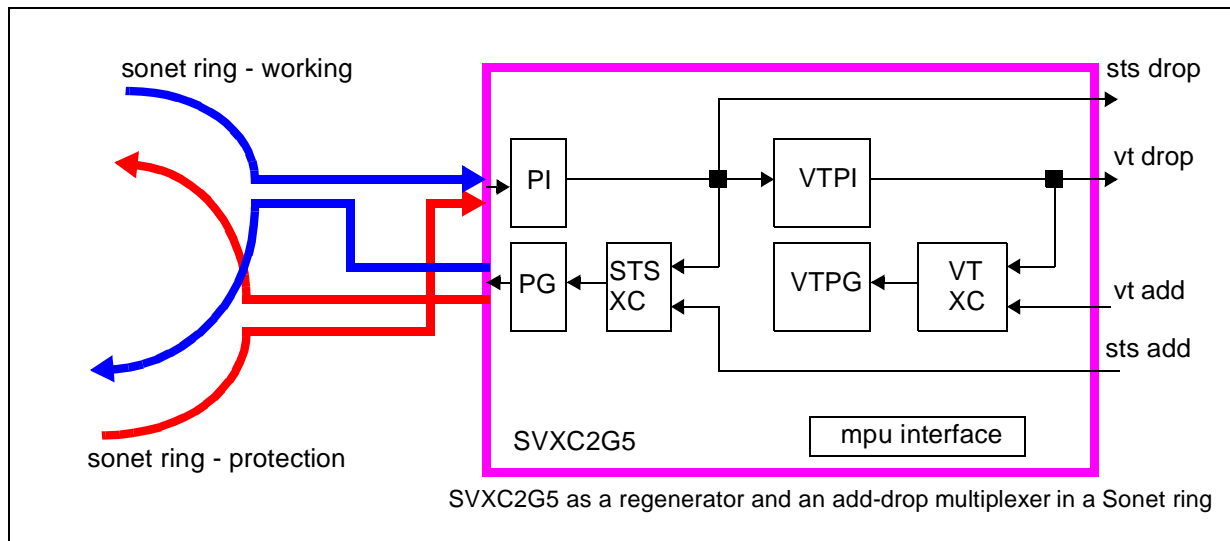


Figure 1 SVXC2G5 typical application in a Sonet ring

Applications

The SVXC2G5 is a versatile cross connect that can be used as a sonet regenerator, repeater or an end user device. A typical application of the SVXC2G5 in a Sonet ring as a regenerator and an add drop multiplexer is shown in Figure 1.

General Description

The SVXC2G5 accepts four STS12 streams. Two of the streams can be from the working channel and the other two can be from the protection channel. The data is framed and the line overhead bytes are monitored. The H1H2 bytes are processed by the pointer interpreter and the path overhead bytes are monitored. The individual STS1 SPEs are then sent to the STS level cross connect or to the VT pointer interpreter or simply dropped at the system side.

The VT pointer interpreter works on a VT group basis. Thus individual groups may carry different VT types. It process the V1V2 bytes and sends the data to the VT cross connect. Also any of the VTs can be dropped at the system side through the TDM bus interface.

In the transmit direction, the received STS1s or VTs can be sent along with added STS1s or VTs, filling in the STS1s or VTs that are dropped in the receive direction. A functional block diagram of the SVXC2G5 is shown in Figure 2.

The TDM interface outputs the time slot number and the corresponding data, and J1 marker. For VTs it outputs the VT group, VT number and the V5 marker.

The V5 byte is optionally monitored in the receive direction and can be generated and inserted in the transmit direction.

Ordering and further Information

To learn more about this or any other Tip cores, contact

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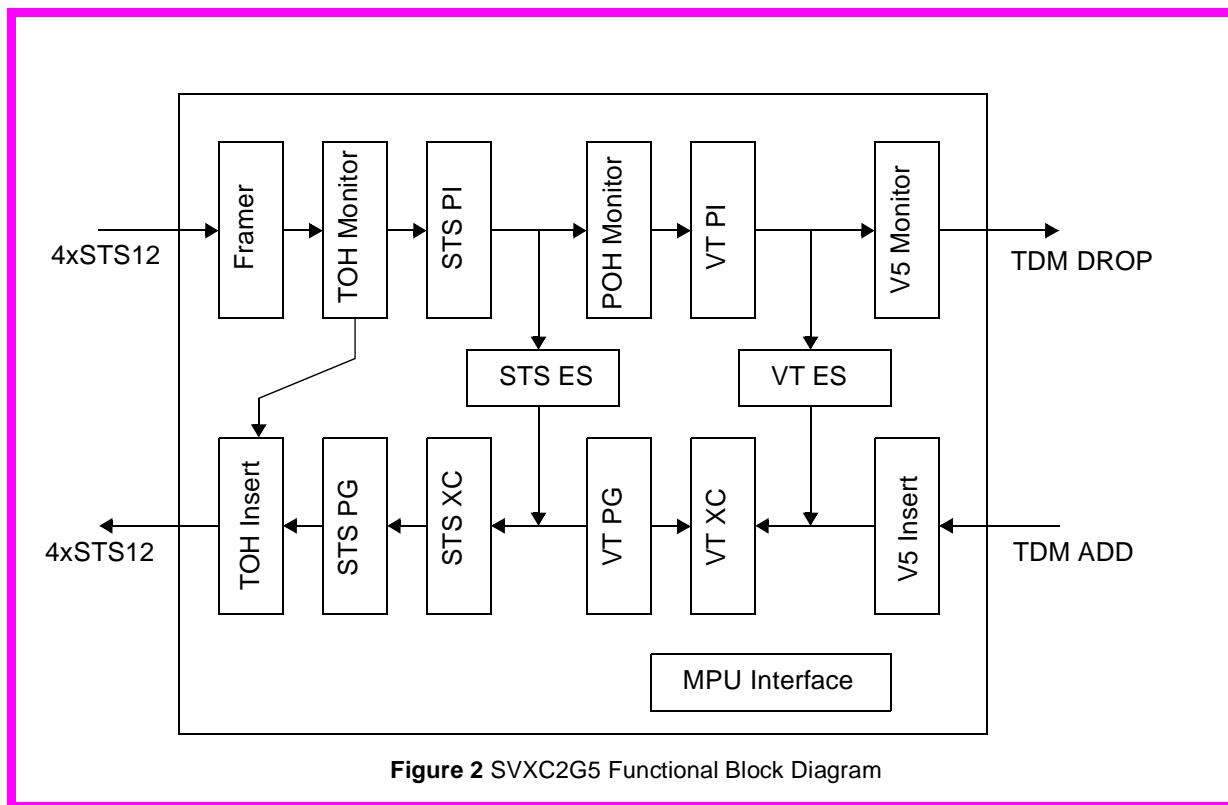


Figure 2 SVXC2G5 Functional Block Diagram