TENESIX INC.

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Low Latency Image Processing Pipeline in a Xilinx or Altera FPGA

Tenesix has developed an FPGA-based Low-Latency Image Processing Pipeline. Available in both Xilinx (Spartan 3A DSP, Virtex-4 SX, Virtex-5 SXT), and Altera families (Cyclone 2, Cyclone 3, Stratix 2, Stratix 3), the Pipeline can be customized to suit many applications which include Medical Imaging, Surveillance and 3-D Sensing.

Sensor Calibration and Correction:
A long-term gain and offset value is subtracted, if necessary, from the incoming pixels to account for variations in temperature or even in between sensors. Sometimes manufacturing variations cause each pixel to respond slightly differently to an input light level. This is corrected by once again, subtracting a gain and offset value on pixel-by-pixel basis (Two-Point Correction). A state-less area ordering filter is used to suppress the effects of defective pixels. If a grid-like effect is seen, Anti-Aliasing filters are used. All this is done to correct and calibrate a sensor. All sensors of course do not need all these modules.

Demosaic:
A demosaicing algorithm is used to interpolate a complete image from partial raw data that is received from a color-filtered image sensor using a Color Filter Array (CFA). Several demosaicing algorithms are available.

Display Pre-Calibration (Gamma Correction, Smoothing & Sharpening):
Sometimes the response of image sensors to light at different wavelengths does not match the human visual system due to the physical characteristics of the materials used. A 3x3 filter is used to manipulate and correct the color representation of the sensor. Gamma correction, a nonlinear operation to code and decode luminance or tristimulus values is used to linearize the response curve of the sensor and the display systems. A sharpening filter is used to pre-correct for the mod-ulation-transfer-function (MTF) of the display and the Contrast Sensitivity Function (CSF) of the user. These filters are used to pre-correct for the nonlinear behavior of the displays.

Display Pipeline (Output Synchronization, Size Adjustment, Interlacing, Overlays & Output Formatting):
The display pipeline synchronizes the sensor rate to the output display rate using external DDR2 memory. When the sensor size does not match the display size, the image is resized to place the image at the center of the display. The image is interlaced and overlays inserted before formatting the output to match the display (DVI, VGA, S-Video, Composite).

Image Processing:
The above described blocks simply calibrate and correct the sensor, pre-calibrate the display, and display the image on a monitor. Customer specific algorithms are inserted in between the sensor pipeline and the display pipeline. These include programmable filters, fixed and adaptive threshold-ing algorithms, and binary filters (Dilation, Erosion, Closing, Opening, Rank).

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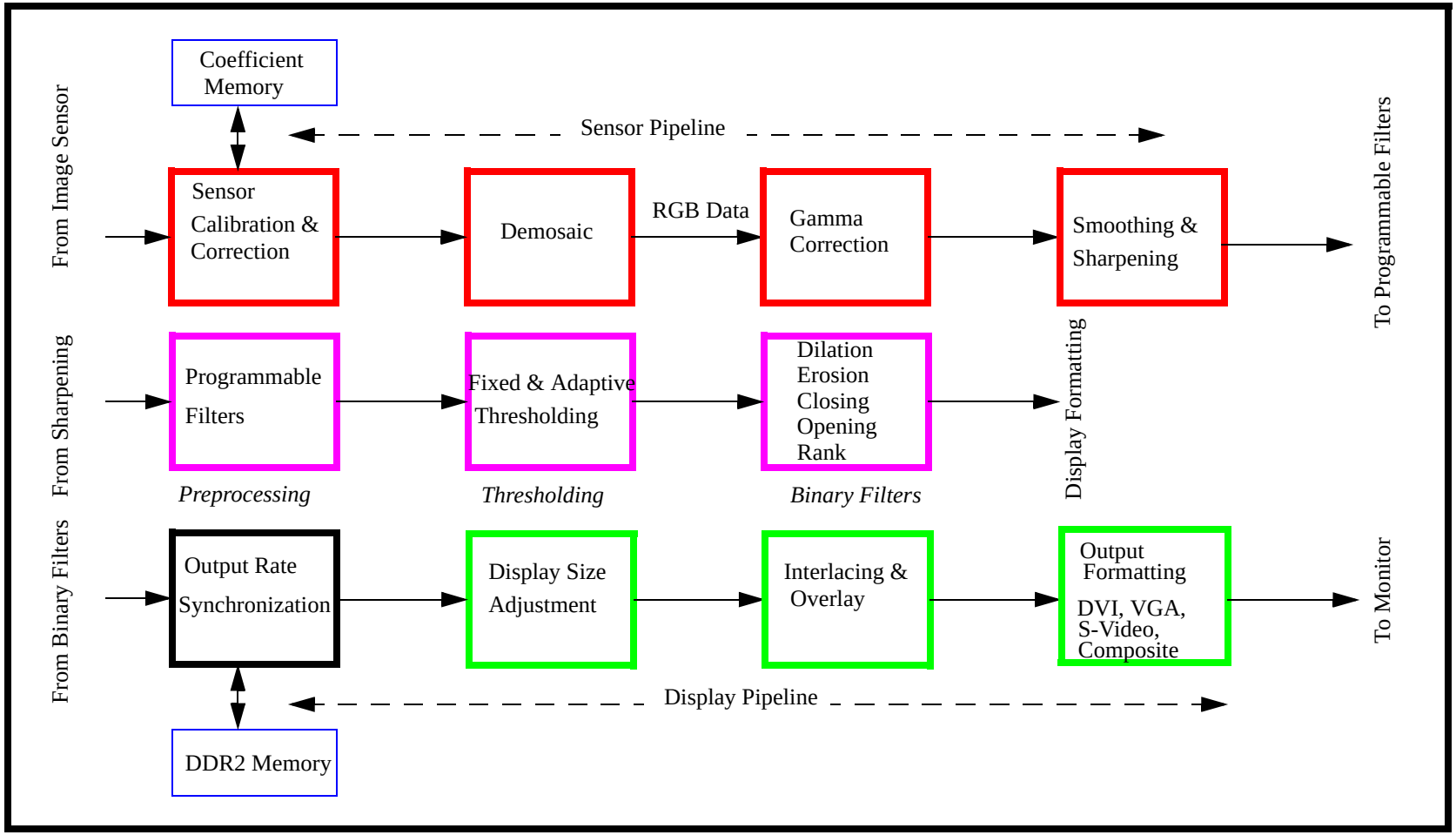
Fig 1: FPGA-Based Low-latency Image Processing Pipeline



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