

2.5Gbps STS48 VC Delay Compensation

1. Features

- Supports four STS12 622 Mbps signals operating as either 1 x STS48 or 4 x STS12
- Supports from 1 to 16 channels each with STS-1/3c (aggregate up to STS48 bandwidth)
- Differential delay compensation of 14 ms up to 254 ms through an off-chip Double Data Rate DRAM
- Selective pass-through for channels which are not virtually concatenated
- Pointer generator compensates the incoming VC payload drift in the transmit direction
- Synchronous/Asynchronous 16-bit address/ 16-bit data micro processor interface
- Input and DDR loop backs for diagnostic purposes
- Simple interface, four 8-bit data operating on a single clock
- Internal single clock of operation
- Implementation on Altera Stratix EP1S25
- Mates with the STM interface of a SONET device through a single-chip back plane transceiver
- Supports Dynamic Bandwidth Allocation algorithm (including LCAS inter operability in Fixed Allocation Mode)

2. Description

The VC2G5F device aligns (differential delay compensation) VC SONET traffic and forwards the data as an aligned VC stream to a SONET device for Path Termination. This device provides a network differential delay compensation of 14 ms to 254 ms on tributaries that are virtually concatenated in an STS-48 bandwidth. It supports up to sixteen individual virtually concatenated channels sharing the STS-48 bandwidth and functions with a network terminal or regenerator equipment. The device is intended to be used along with a SONET device and a back plane transceiver or any other device supporting virtual concatenation.

3. Product Applications

The device interfaces with the STM interface of the SONET device through a backplane transceiver. The incoming STM data (STS48/4xSTS12) which contains virtually concatenated channels is first passed through the transceiver device. The back plan transceiver performs the Clock Data Recovery (CDR) function, Deserializes (Rx)/ Serializes(Tx) the data (SerDes), frames on this data and transfers it to a single system clock. The received parallel (8-bit data and 1-bit parity) data is sent to the VC2G5F. Within the VC2G5F, time slots which are virtually concatenated are aligned (to perform delay compensation) and time slots which are not virtually concatenated are turned around and sent back to the SONET device via the back plane transceiver. A typical application of the device is shown in Figure 1.

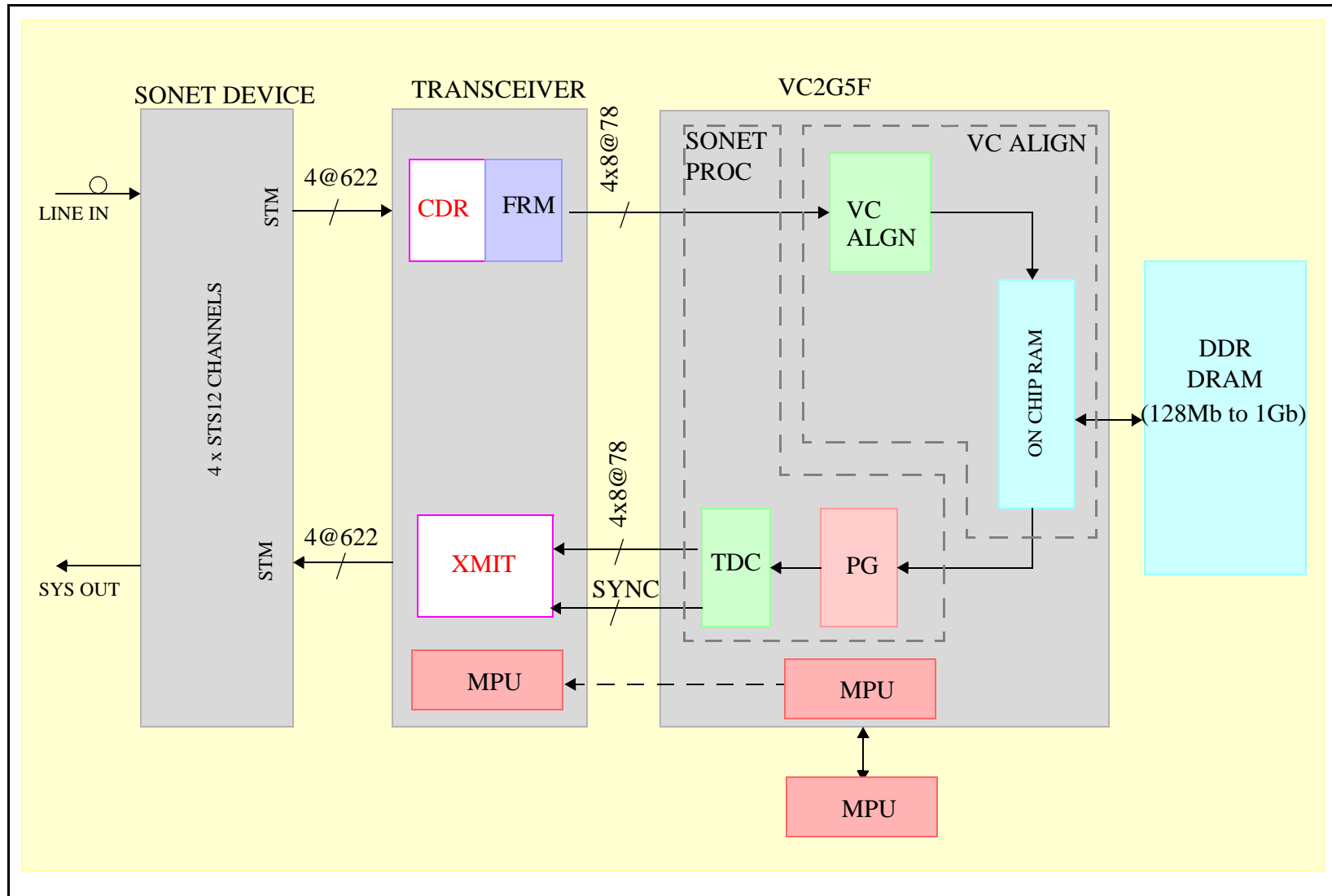


Figure 1. VC2G5F Network Application Block Diagram